

Variation immune system for sub-threshold operation

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ABSTRACT

In this paper, we present an immune system methodology to deal with variations in sub-threshold operation regime. Making use of the Razor approach our system detects circuit level timing errors and tunes the supply voltage accordingly.

1. INTRODUCTION

During the last 12 years, it has been proven the capabilities and potential of the sub-threshold regime to develop Ultra Low Power ICs. Researchers have been developing all kind of applications in the Sub-threshold regime, i.e. a FFT processor that runs on 180mV[1], a Sub-threshold FPGA[2], a Sub-threshold ring oscillators at 80mV[3], a 256kb memory chip in Sub-threshold region below 400mV[4], and ultimately a wireless Wearable Body Sensor Node running on harvested energy consuming 19uW of energy[5]. However the last obstacle to make this technology fully commercial is the tremendous sensitivity of the circuits to variations in process, voltage and temperature (PVT), which severely affect the delay in combinational circuits and thereby affect the product yield for timing violations. In general the circuits are designed under the fixed voltage – fixed frequency paradigm which does not account for the increased sensitivity to variation in sub-threshold regime. This is exemplified in Figure 1 and 2. The first data transition meets the setup time of the flip-flop and the data is latched correctly. However during the second data transition there is a timing violation, so the flip-flop is unable to latch the data correctly which is an error.



Figure 1 Combinational Logic plus data flip flop. Typical example of sensitive circuit to variation.

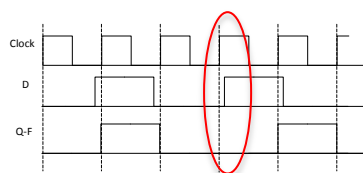


Figure 2 Timing diagram showing the effects of variation and timing violation.

In this paper we present a variation immune system based on the razor approach. In general the systems are designed under the fixed voltage – fixed frequency paradigm. With our approach the chip is able to tune the operation point on the fly accounting for global and local variations, therefore increasing the yield of the product. For the purpose of this paper we use a 3 bit ripple carry adder as our combinational logic.

2. RAZOR APPROACH

The concept of razor is illustrated in Figure 3. Each flip-flop in the critical path of the system is augmented with a shadow latch. Which is controlled by a delayed clock[6].

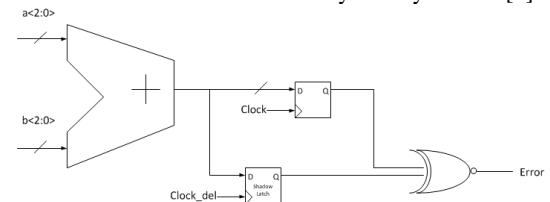


Figure 3 Razor concept using the 3 bit ripple carry adder.

We illustrate the razor operation in the time diagram in Figure 4. If the data does not meet timing, as shown in the second transition, although the flip flop does not latch the data correctly, the latch does. Then the output of the flip flop and the latch is compared and the error signal is generated if they are not the same.

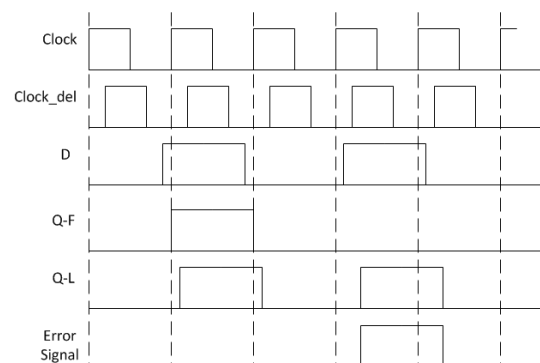


Figure 4 Time diagram showing Razor operation

3. Dummy DVS

With the error signal produced, the voltage of the system is controlled. We implement a simplified dummy DVS system. This system includes a voltage controller that detects that an error is generated. Once the error is detected the voltage controller shifts the one hot output which controls a set of PMOS headers[7] as shown in Figure 5.

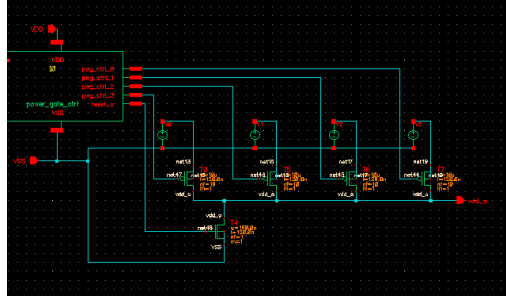


Figure 5 DVS approach

4. Complete Variation Immune System proposed

A Diagram of the overall system is shown in Figure 4 below. For dynamic voltage scaling, we made use of PMOS headers in the voltage controller block to switch from the voltage from a lower to a higher level.

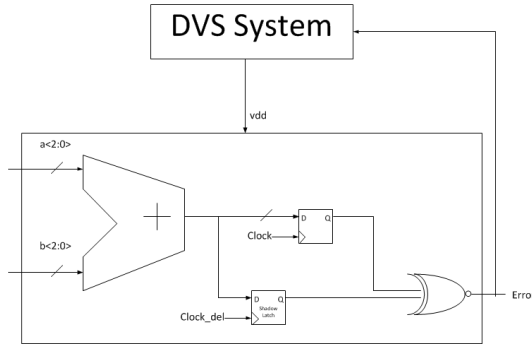


Figure 6. Complete Block diagram of the Variation Immune System proposed

5. OPERATION AND METHODOLOGY

The circuit was designed to operate at three different frequencies so that it can handle three different workloads. The table below shows the operation frequencies and the voltage range.

Voltage Range (V)	Frequency
0.4 – 0.5	100 kHz
0.5 – 0.7	200 kHz
0.7 – 1	40 MHz

Table 1: Operational frequencies

For 0.4-0.5V, we increase the voltage in steps of 0.25V. As we move to higher voltages, the increase in performance obtained from finer increase in voltages was seen to be lesser. Hence, from 0.5-0.6 V, we increase with steps of 0.5V and from 0.7-1 V we increase in steps of 1V. In effect, we have 4 levels of granularity in each range of operation.

For testing, we initially start with the lowest operating voltage for a frequency range. As it detects errors, the circuit attempts to compromise for the delay changes of the combinational circuit by incrementing the voltage in steps. As we increase the voltage, we see that the errors are eliminated and the circuit reaches a stable voltage of operation when no further errors are encountered.

Typically, designers have to work on an extensive corner analysis to select a supply voltage. Quite an amount of extra margin has to be implemented into the circuit design/sizing for worst-case scenario. For sub-threshold operation, the variability might increase and hence the typical voltage margins required will be higher. But the case in which variability never occurs or is rare, the system could be operated at a lower voltage with a great amount of energy savings. For our design, it was made sure that the test circuit operates at the typical corner case. Effort was taken to make the razor circuits robust and functional across different corners and supply voltages.

6. RESULTS

An extensive Monte-Carlo analysis was performing on the circuit for the three frequencies at three temperatures of operation (T=20,27,100C).

To begin with, the worst-case power consumption of the Razor circuit was close to 1.5nW for a voltage of 0.4V. Hence, the overhead of the Razor approach in a bigger system will not be tremendous, provided the fact that this will be implemented only for critical and near-critical paths.

Following are a few pie charts, which are representative of the results of our Monte-Carlo analysis.

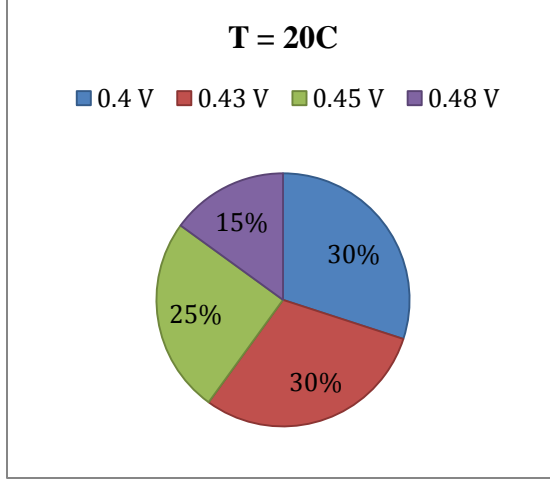


Figure 7 Percentage of chips working at various voltages, T=20C, f=40MHz

From the above plot in Figure 7, we see the percentage of chips, which would effectively be functional at different supply voltages. A 30% works at the lowest possible voltage and a 15% at the highest possible voltage. Typically, the designers may design the circuit to be functional at 0.45V. From our results, we see that roughly 60% of the chips can be made to work at less than 0.45 V, which is a tremendous savings of power at a very less overhead of the power consumed by the razor circuit. Table 2 represents the power savings we see.

Frequency	Voltage (V)	% Savings W.r.t highest Voltage
100 kHz	0.4	31.81%
	0.425	21.99%
	0.45	14.21%
	0.475	Highest voltage
200 kHz	0.5	38.21%
	0.55	25.49%
	0.6	18.32%
	0.65	Highest voltage
40 MHz	0.7	42.49%
	0.8	29.24%
	0.9	15.08%
	1	Highest voltage

Table 2: Power savings for different frequencies

7. CONCLUSION

In this work we have shown that it is possible to increment the yield for ICs operating in the sub-threshold regime. Using the Razor approach, we showed that VDD can be adapted on the fly to account for PVT variations. With our approach, chips that otherwise would have been discarded for timing violations, now adjust their operation point to meet setup and hold time and be fully functional increasing the yield metric.

7. Acknowledgments

To all the people who helped here. It is impossible to count all but they know it in their hearts!

8. References

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